REMARKS:

RESPONSE TO CLAIM OBJECTION

Claim 28 is objected to in the Office Action. Since the specification states in line 18 on page 9, "such as speech decoders using....." Applicants have amended claims 28 to read "wherein the speech decoder uses a coding scheme....."

RESPONSE TO CLAIMS REJECTION UNDER 35 U.S.C. 112

Claims 17-28 were rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. More specifically, the Examiner determined that the limitations in claims 17 of "a fist-stage decoding circuit" and "a second-stage circuit" were not described in the original specification.

The paragraph of the specification appearing in lines 14-16 on page 3 reads, "The first switch SW1 and second switch SW2 are switches for switching the signals to be processed SPC so as to be supplied to the latter-stage circuits through the emphasis processing portion 15, or so as to be supplied to the latter-stage circuits through the bypass BP." (underlines added). The specification distinguishes between the circuits located downstream of the emphasis processing portion 15 and the circuit located upstream of the portion 15. The specification distinguishes the downstream and upstream circuits by naming the downstream circuits "the latter-stage circuits". Relying on this disclosure in the specification, in the previous amendment, Applicants defined in claim 17 the "upstream circuits" as a "first-stage circuit" and the "downstream or latter-stage circuits" as a "second-stage circuit". Thus, the terms "a fist-stage circuit" and "a second-stage circuit" recited in claim 17 are fully defined and supported by the disclosure of the specification.

Also, the present invention is drawn to a speech decoder. Each element in the circuitry described in the specification and illustrated in the attached drawings

performs a decoding function. Of course, the above former and latter-stage circuits both perform decoding functions. Therefore, using the terms "a fist-stage decoding circuit" and "a second-stage decoding circuit" conforms to the disclosure of the specification and the attached drawings.

Furthermore, claims 17 not just recites "a first-stage decoding circuit" but recites "a first-stage decoding circuit that generates excitation vectors from the received parameters". There can be found in Fig. 2, for instance, "adaptive code vector decoder" (22), "fixed code vector decoder" (23) and "gain decoder" (24) (underlines added) located upstream of the adaptive preprocessing filter 25. The functions of these decoders 22, 23 and 24 are well known by one of ordinary skill in the LP speech coding area. As discussed in detail in the specification (see page 5), these decoders generate excitation vectors to be used to drive a speech synthesis filter to reconstruct a speech.

Likewise, claim 17 not just recites "a second-stage decoding circuit" but recites "a second-stage decoding circuit that performs a speech synthesis, using the excitation vectors, to obtain a reconstructed speech". There can be found in Fig. 2, for instance, "LP synthesis portion" (28) (underline added). Again, the function of the LP synthesis filter is well known by one of ordinary skill in the art. In fact, the specification states in lines 16-17 on page 6, "The LP synthesis filter 28 is a device which performs an LP synthesis based on the excited signal SEXC and the LSP coefficient CLSP to reconstruct the speech signal SSPC" (under line added).

For the reasons set forth above, the terms "a first-stage decoding circuit" and "a second-stage decoding circuit" are fully defined and described in the application. Applicants respectfully request that the claim objection be withdrawn.

RESPONSE TO CLAIM REJECTION UNDER 35 U.S.C. 102

Claims 17-23, 27-32 and 36 were rejected under 35 U.S.C. 102(e) as being

anticipated by SALAMI et al. The Examiner determined that the vector modifier recited in claim 17 corresponded to the filter $P(z) = 1/(1-\beta z^{-T})$ discussed in SALAMI et al. Further, referring to the discussion in SALAMI et al. regarding the concealment operation, the Examiner indicated in the Office Action that the filter was a function of variables gain β and integer part of pitch lag T and the gain and pitch lag would be changed during the concealment based on the condition of the detected frame errors, so that the replacement excitation are vary, which is interpreted as a variable degree of enhancement.

First of all, in determining that the filtering effect performed by the above P(z) varied as a count of error frames increases, the Examiner seems to rely on Equation (53) of SALAMI et al. appearing in the right column on page 125 of SALAMI et al. Please note that Equation (53) defines the way that the averaged quantized gain prediction-error is attenuated. As discussed in the left column on page 123 of SALAMI et al., the averaged quantized gain prediction-error is used to predict the fixed-codebook gain. On the other hand, β in P(z) is the adaptive-codebook gain. SALAMI et al. is silent about how β varies in accordance with the concealment operation.

Second, the Examiner indicated that the pitch lag T changed during the concealment. But there is nothing in SALAMI et al. that indicates that the pitch lag T changes during the concealment.

In order to more clearly define the subject matter of the present invention, Applications have amended claim 17 as above, which is produced below:

17. A speech decoder that decodes parameters received in frames and reconstructs a speech based on the received parameters, comprising:

a first-stage decoding circuit that generates excitation vectors from the received parameters:

a second-stage decoding circuit that performs a speech synthesis, using the excitation vectors, to obtain a reconstructed speech;

an adaptive preprocessing filter, located between the first-stage and second-stage circuits, that emphasizes, to a degree, a harmonic component of at least one of the excitation vectors; and

an error frame counter that counts successive error frames that contain a transmission error, the error frame counter operably connected to the adaptive preprocessing filter to decrease the degree of emphasis performed thereby as a count of the successive error frames increases, wherein the error frame counter disables the adaptive preprocessing filter to effect zero emphasis on the at least one of the excitation vectors when the count of the successive error frames reaches a predetermined number.

The adaptive preprocessing filter recited in claim 17 as amended corresponds, for instance, to the filter P(z) discussed in SALAMI et al. and functions to emphasis a harmonic component of at least one of the excitation vectors. For the support of this claim limitation, please refer to the paragraph in lines 18-20 on page 5 of the present specification, which reads, "The adaptive preprocessing filter 25 is a device which functions as an emphasizing process means for emphasizing the harmonic components of the decoded original fixed code vector FCV0, and outputs the result as a fixed code vector FCV."

As indicated by the Examiner in the Office Action, SALAMI et al. is silent about "the error frame counter that counts successive error frames" recited in claim 17. Further more, as defied in amended claim 17, the error frame counter functions to disable the adaptive preprocessing filter when the count of the successive error frames reaches a predetermined number. In SALAMI et al., P(z) never becomes zero no matter what values β and T take. Since there is nothing

in SALAMI et al that discloses or teaches the error frame counter, claim 17 as amended above is not anticipated by SALAMI et al.

RESPONSE TO REJECTION UNDER 35 U.S.C. 103

Claims 24-26 and 33-35 were rejected under 35 U.S.C. 103(a) as being unpatentable over SALAMI in view of MANO et al. The Examiner indicated, "SALAMI does not expressly disclose that the error detector counts a number of successive frames that contain a transmission error. However, this feature is well known in the art as evidenced by MANO, who discloses flag group (S2, S1, S0) for counting the number of consecutive error frames."

Claim 17 as amended above recites the error frame counter that decreases the degree of emphasis by the adaptive preprocessing filter as a count of the successive error frames increases and that disables the adaptive preprocessing filter to effect zero emphasis when the count of the successive error frames reaches a predetermined number. Neither SALAMI nor MANO discloses the error frame counter that functions to disable the adaptive preprocessing filter when the count of the successive error frames reaches a predetermined number. MANO counts successive error frame, but the count is used for determining whether or not there was an error in the past. In MANO, the number in the count has no particular significance. As evidence by the process illustrated in Fig. 5 of MANO, the determinations made are all to decide whether the count is zero or non-zero. MANO does not look to any specific number. In contrast, in the present invention, a specific number of the count by the error frame counter has more significance than other numbers, and, when the error count reaches the specific number, an action is triggered to decrease the degree of emphasis and ultimately disable the adaptive preprocessing filter. Therefore, claim 17 as amended above should be patentable over SALAMI and MANO.

Respectfully submitted,

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